

Appl. No. 10/758,348  
Amdt. dated September 16, 2004  
Reply to Office Action of July 6, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend the claims as follows:

Claims 1-5 (canceled)

6. (currently amended): A ~~type~~-very long instruction word (VLIW) memory (VIM) direct memory access (DMA) apparatus comprising:

a plurality of VLIW slot function units;

a partitioned VLIW memory (VIM) having a separate VIM section per VLIW slot function unit, each separate VIM section having a plurality of memory locations for storing slot function unit instructions;

a DMA interface receiving a data packet having a plurality of short instruction words (SIWs); and

~~a DMA-very long instruction word (VLIW) line buffer; and~~

a VIM load controller for selecting a separate VIM section and separately selectively controlling the loading of at least one SIW from the received plurality of SIWs into each the selected separate VIM section.

7. (original): The apparatus of claim 6 wherein each separate VIM section has two ports allowing simultaneous read and write accesses.

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8. (currently amended): The apparatus of claim 6 wherein said ~~line buffer receives and temporarily stores a data packet~~ plurality of SIWs comprising:

a load/modify VLIW memory address (LV2) instruction SIW specifying a separate VIM section, a number of slot function SIWs (SFSIW) to be loaded constituting a block of SFSIW, and a starting address of the block of SFSIW where the SFSIW are to be loaded in the specified separate VIM section; and

a plurality of at least one short instruction words (SIWs) SFSIW associated with the LV2 SIW.

~~constituting a specified functional VIM portion to be loaded at an address specified in the LV2 instruction.~~

Claims 9-12(canceled)

13. (currently amended): A ~~type of~~ method for providing direct memory access (DMA) loading of a partitioned very long instruction word (VLIW) memory (VIM) ~~direct memory access (DMA)~~, said method comprising the steps of:

~~storing a DMA very long instruction word (VLIW) line buffer;~~

receiving a DMA data packet having a plurality of short instruction words (SIWs);

utilizing a VIM load controller for separately controlling the loading of each separate VIM section in a partitioned ~~VLIW memory (VIM)~~, the partitioned VIM having a separate VIM section per VLIW slot function unit; and

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~~selectively routing the appropriate portions of said VLIW from said line buffer at least one SIW from the received plurality of SIWs to said a separate VIM sections on a DMA interface selected by the VIM load controller.~~

14. (currently amended): The method of claim 13 wherein each separate VIM section has two ports allowing simultaneous read and write accesses, and the method further comprises the step of separately providing each of the two ~~parts~~ ports for each separate VIM section ~~its own a~~ read address, a write address, and associated read or and write control signals.

15. (currently amended): The method of claim 13 further comprising the step of receiving ~~and temporarily storing in said line buffer~~ a plurality of data packets, each data packet comprising a load/modify VLIW memory address (LV2) instruction SIW, and a plurality of at least one short instruction words (slot function SIWs) (SFSIW) associated with the LV2 SIW, the LV2 SIW constituting specifying a specified functional separate VIM portion section to be loaded at an address specified in by the LV2 instruction SIW.

16. (canceled)

17. (currently amended): A very long instruction word (VLIW) memory (VIM) direct memory access (DMA) apparatus comprising:

a plurality of functional execution units, each functional execution unit performing a distinct operation;

a VLIW memory (VIM) having a plurality of VIM sections, each VIM section storing short instructions words (SIWs) corresponding to each one of the plurality of functional execution units, each VIM section associated with a one of the plurality of functional execution

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units, each stored ~~instruction-SIW being~~ selectable from any VIM section for parallel execution with any other stored ~~instruction-SIW~~ associated with a different functional execution unit of the plurality functional execution units;

a DMA ~~very long instruction word (VLIW) line buffer~~ interface for receiving a data packet having a plurality of ~~instructions-SIW~~ to associated with a VIM section; and

a VIM load controller for separately controlling the loading of ~~each received instruction at~~ least one SIW of the received plurality of instructions-SIW into a separate VIM section.

18. (previously presented): The apparatus of claim 17 wherein each of the plurality of VIM sections has two ports allowing simultaneous read and write accesses.

19. (currently amended): The apparatus of claim 17 wherein said ~~line buffer temporarily stores the data packet~~ plurality of SIWs comprising comprises:

a load/modify VLIW ~~memory address (LV2) instruction-SIW specifying a separate VIM section, a number of slot function SIWs (SFSIW) to be loaded constituting a block of SFSIW, and a starting address of the block of SFSIW where the SFSIW are to be loaded in the specified separate VIM section; and~~

a plurality of ~~short instruction words (SIW), SFSIW associated with the LV2 SIW.~~

~~each short instruction word of the plurality of short instruction words loaded into a VIM section at an address specified in the LV2 instruction.~~

20. (currently amended): A method for loading very long instruction word (VLIW) memory (VIM) through a direct memory access (DMA) controller, said method comprising:

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providing a VLIW memory (VIM) having a plurality of VIM sections, each VIM section storing short instruction words (SIWs) corresponding to a functional execution unit of a plurality of functional execution units, each stored ~~instruction~~ SIW selectable from any VIM section for parallel execution with any other stored ~~instruction~~ SIW associated with a different functional execution unit;

receiving a data packet having a plurality of ~~instruction~~ SIWs ~~into a line buffer~~ associated with a VIM section; and

selectively loading ~~each instruction~~ SIWs of the received plurality of instructions from said line buffer to in each corresponding the VIM section associated with the received data packet of the plurality of VIM sections by utilizing a VIM load controller.

21. (currently amended): The method of claim 20 wherein each separate VIM section has two ports allowing simultaneous read and write accesses, and the method further comprises:

separately providing each of the two ~~parts~~ ports for each separate VIM section ~~its open a~~ read address, a write address, and associated read or and write control signals.

22. (currently amended): The method of claim 20 further comprising:  
~~temporarily storing~~ receiving in said line buffer a plurality of data packets, each data packet  
 comprising a load/modify VLIW ~~memory address (LV2) instruction~~ short instruction word (SIW)  
 and a plurality of ~~short instruction words (slot function SIWs) (SFSIW)~~ associated with the LV2  
SIW, wherein the selectively loading step loads each VIM section sequentially, for each data  
 packet, wherein the LV2 SIW specifies the separate VIM section and the starting address of each  
 VIM section is determined by the ~~addresses~~ fields contained in the LV2 ~~instruction~~ SIW.

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23. (new): The apparatus of claim 8 wherein the SFSIW's associated with the LV2 instruction are individually loaded into the specified separate VIM section.

24. (new): A very long instruction word (VLIW) memory (VIM) direct memory access (DMA) apparatus comprising:

- a plurality of functional execution units;
- a partitioned VIM having a plurality of VIM sections, each VIM section storing short instruction words (SIW's) corresponding to one of a plurality of functional execution units;
- a local data memory for storing a DMA data packet having at least one SIW associated with a VIM section; and
- a VIM load instruction specifying an operation that causes at least one DMA data packet SIW to be read from the local data memory and be loaded in a specified VIM section.

25. (new): The apparatus of claim 24 wherein the VIM load instruction further specifies a start address associated with the DMA data packet and a number of instructions in a data packet.